FIG. 1

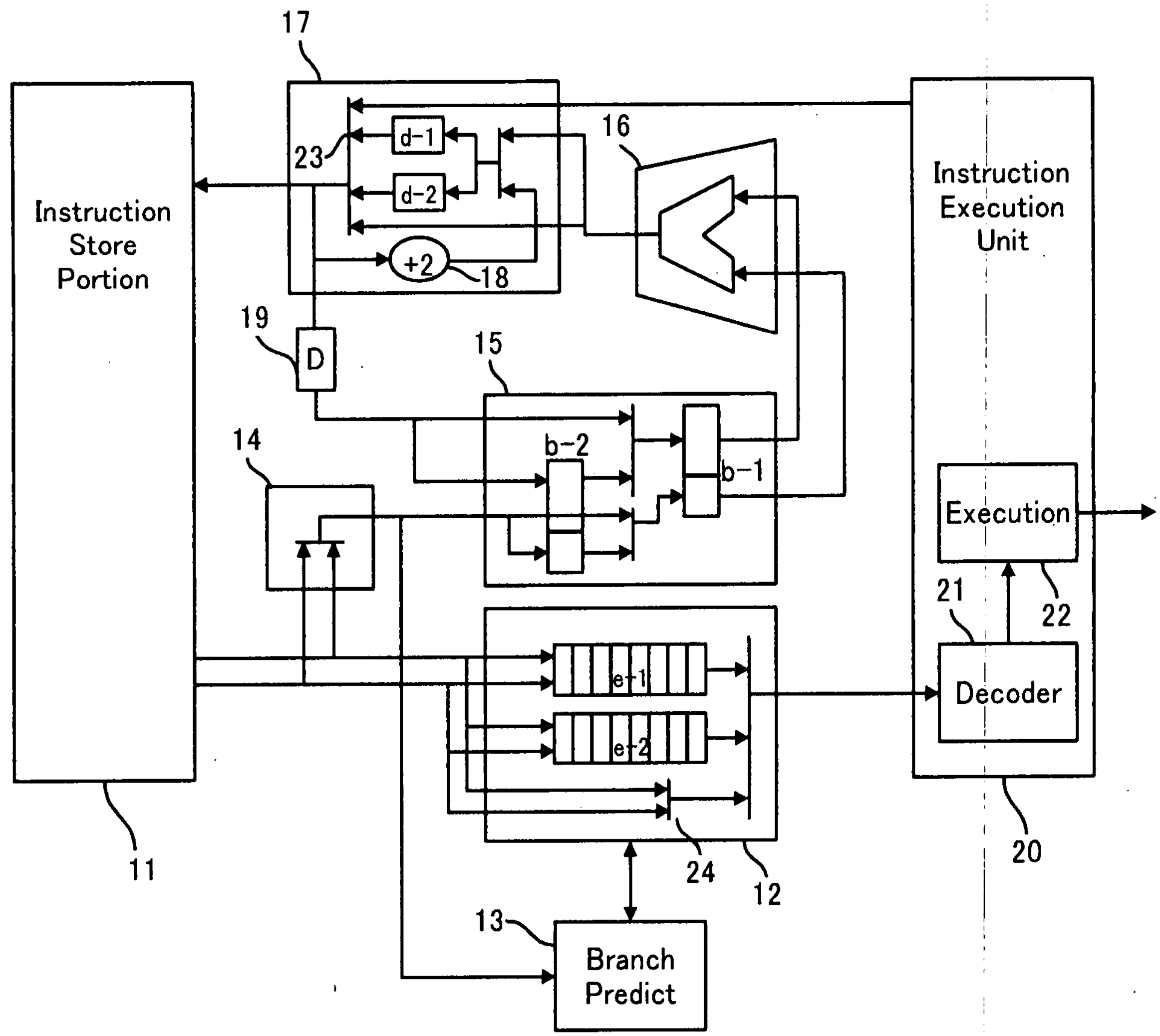

FIG. 2

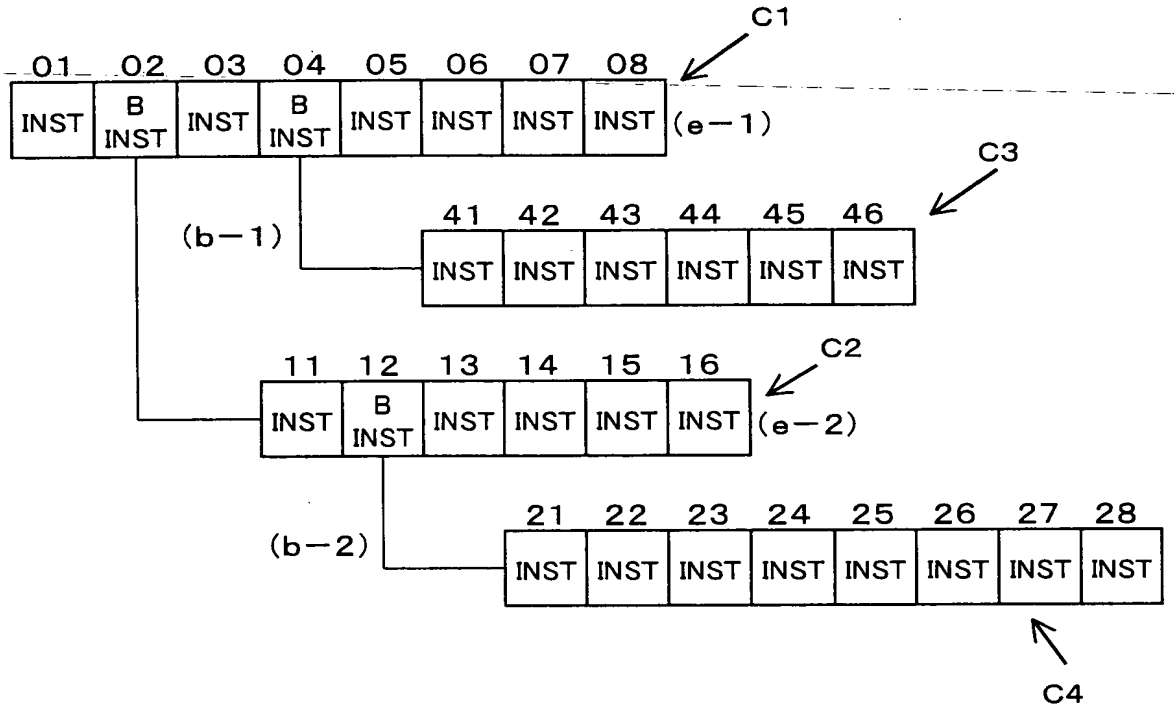

FIG. 3

Instruction Address	Instruction
01	Condition Determination Instruction
02	Condition Branching Instruction (branch to address 11)
03	Condition Determination Instruction
04	Condition Branching Instruction (branch to address 41)
05	Arithmetic Instruction
06	〃
07	〃
08	〃
11	Condition Determination Instruction
12	Condition Branching Instruction (branch to address 21)
13	Condition Determination Instruction
14	Condition Branching Instruction (branch to address 51)
15	Arithmetic Instruction
16	〃
21	Condition Determination Instruction
22	Condition Branching Instruction (branch to address 31)
23	Condition Determination Instruction
24	Condition Branching Instruction
25	Arithmetic Instruction
26	〃
27	〃
28	〃
31	Condition Determination Instruction
32	Condition Branching Instruction
33	Condition Determination Instruction
34	Condition Branching Instruction
41	Condition Determination Instruction
42	Condition Branching Instruction (branch to address 61)
43	Arithmetic Instruction
44	〃
45	〃
46	〃
51	Arithmetic Instruction
52	〃
53	〃
54	〃
55	〃
61	Arithmetic Instruction
62	〃
63	〃
64	〃
65	〃
66	〃

FIG. 4

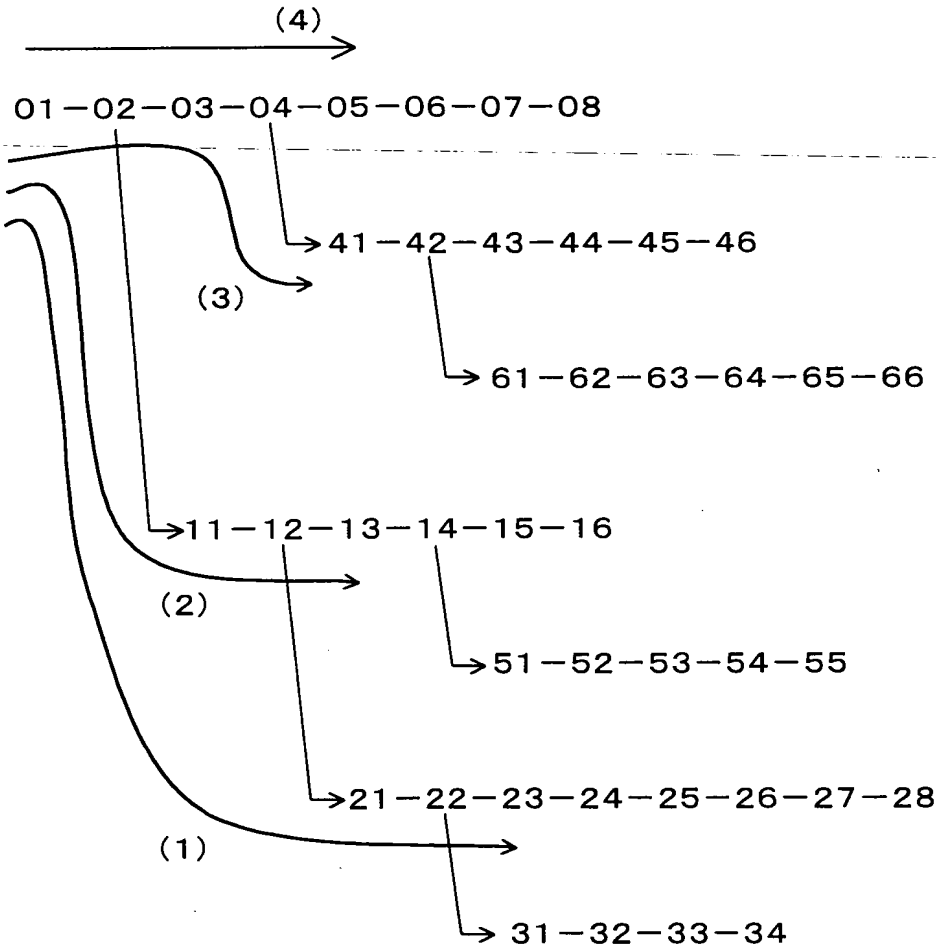

FIG. 5

Branching Route (1)

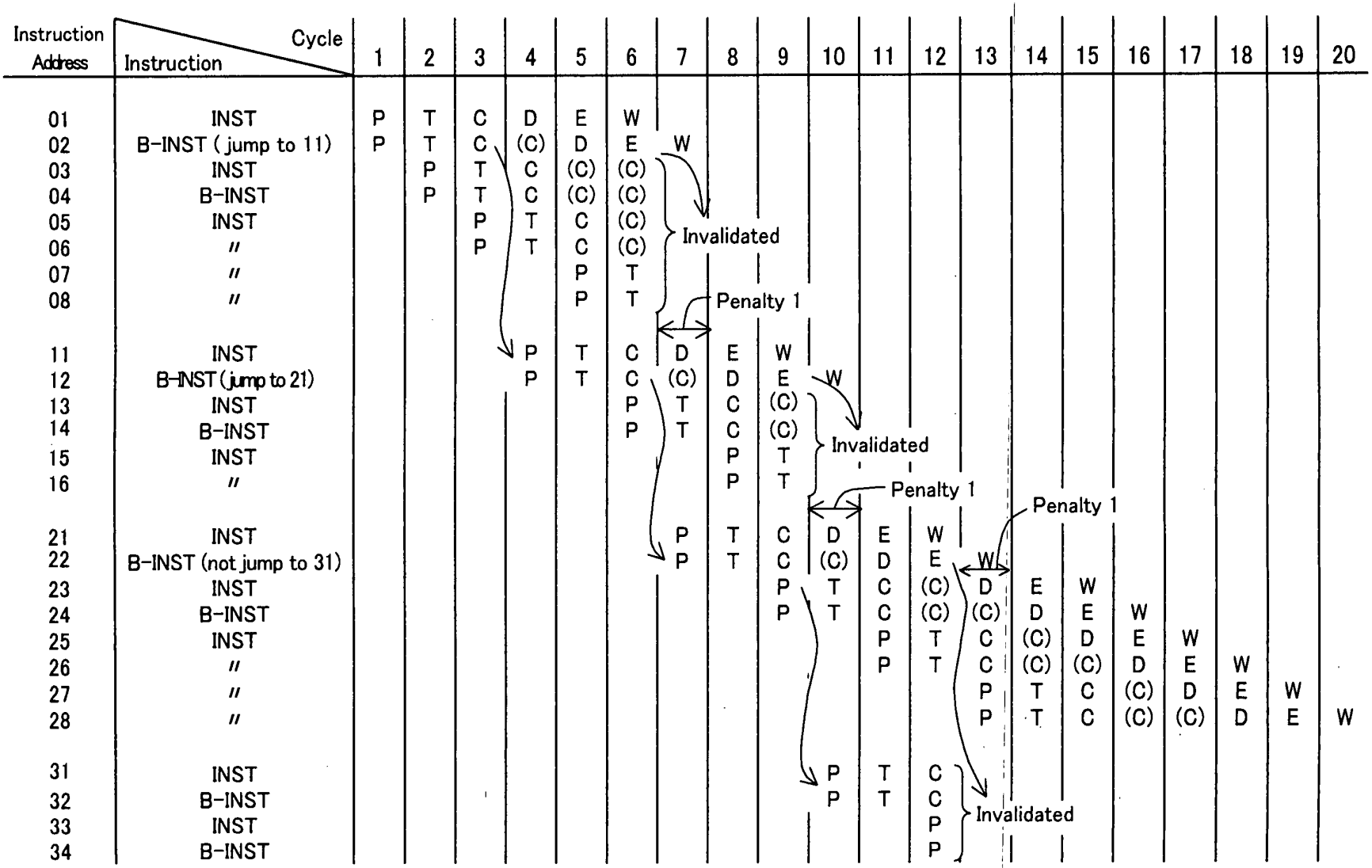

FIG. 6

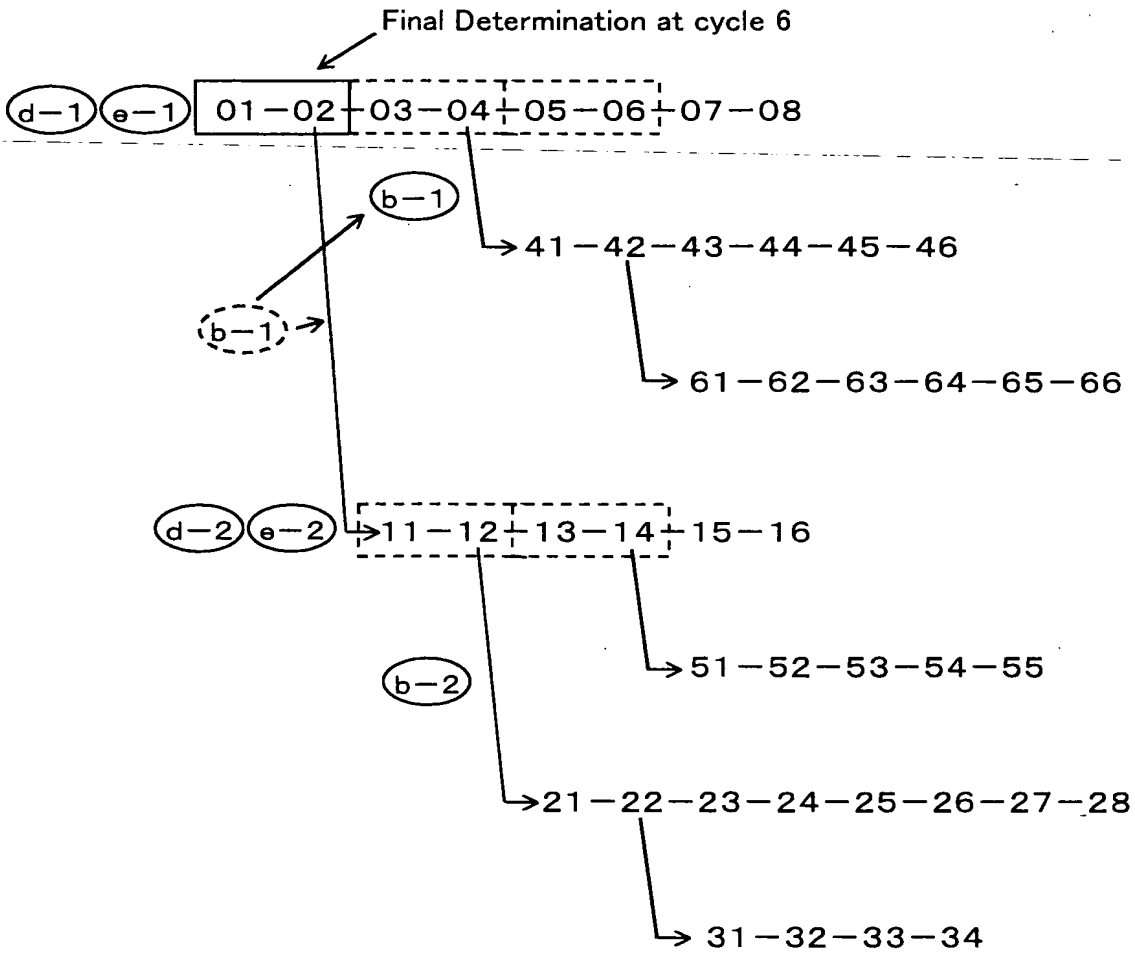
At Cycle 3 for Branching Route (1)
Final Determination at cycle 6
d−1
e−1
01−02
03−04
05−06
07−08
b−1
41−42−43−44−45−46
b−1
61−62−63−64−65−66
d−2
e−2
11−12
13−14
15−16
51−52−53−54−55
b−2
21−22−23−24−25−26−27−28
31−32−33−34

FIG. 7

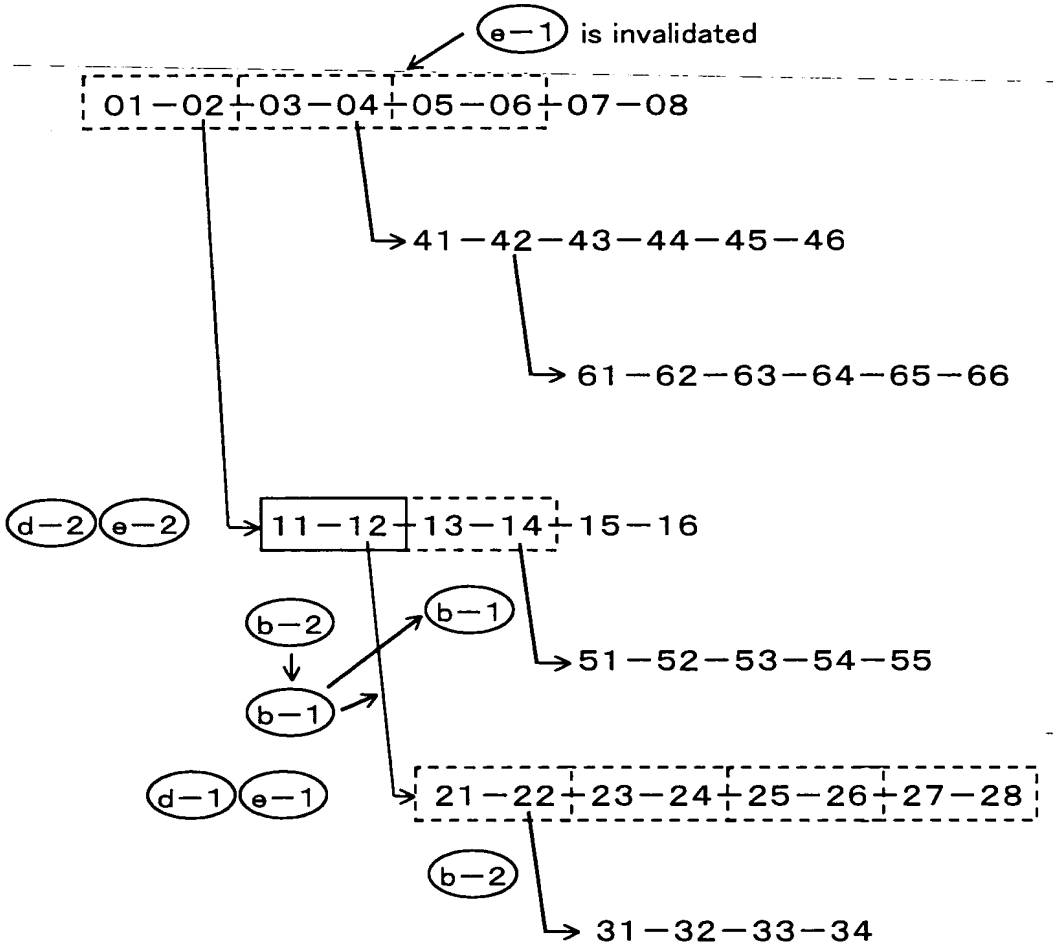

FIG. 8

At Cycle 9 for Route (1)

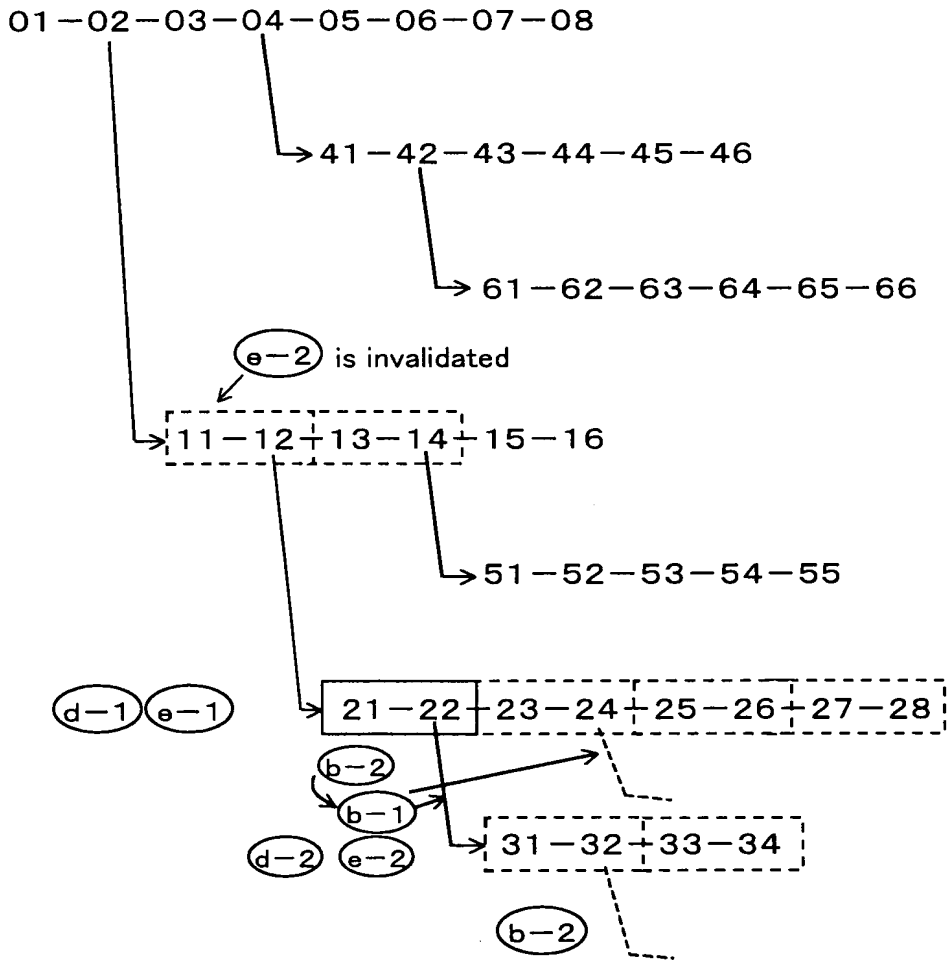

FIG. 9

Branching Route (2)

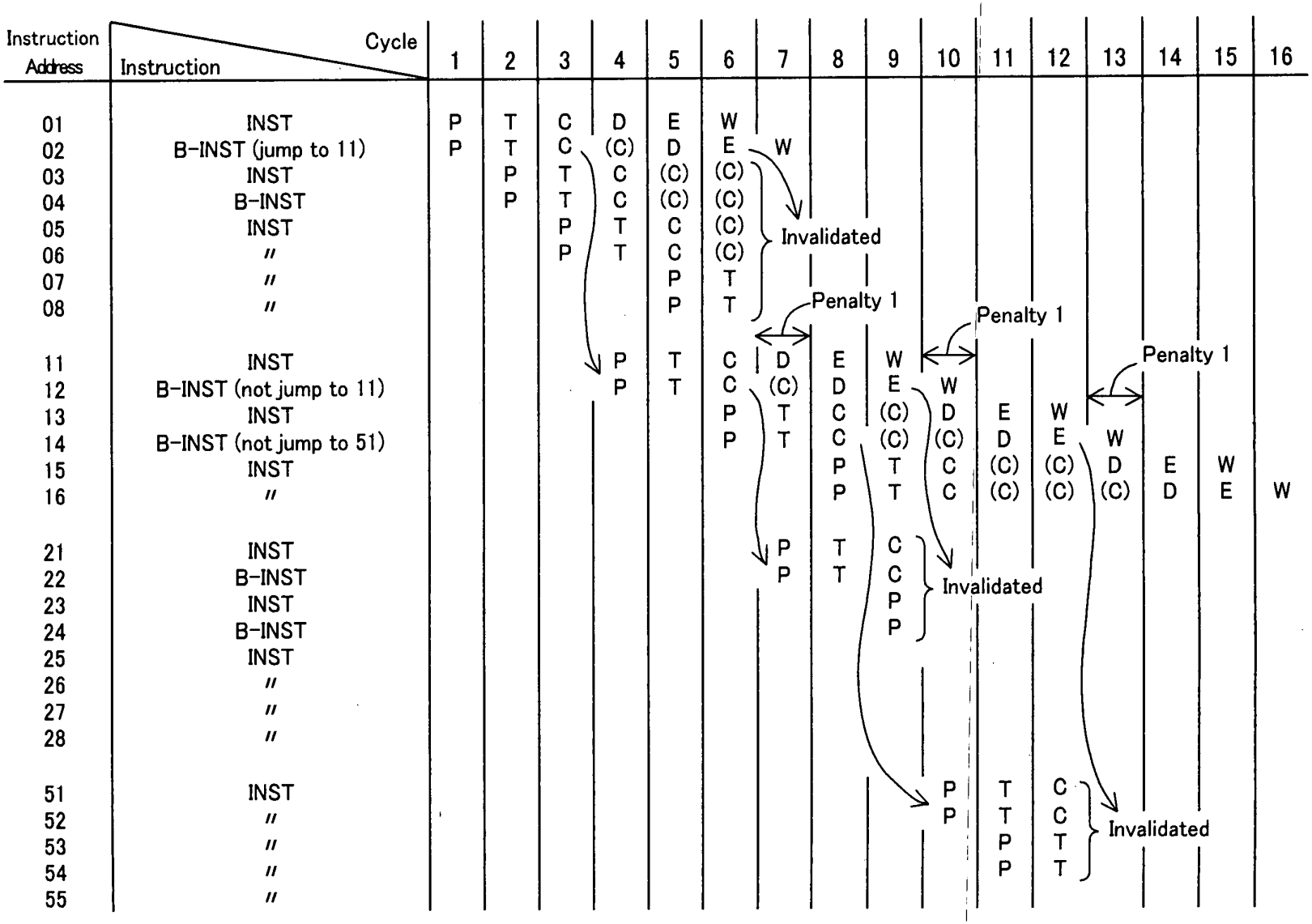

FIG. 10

Branching Route (3)

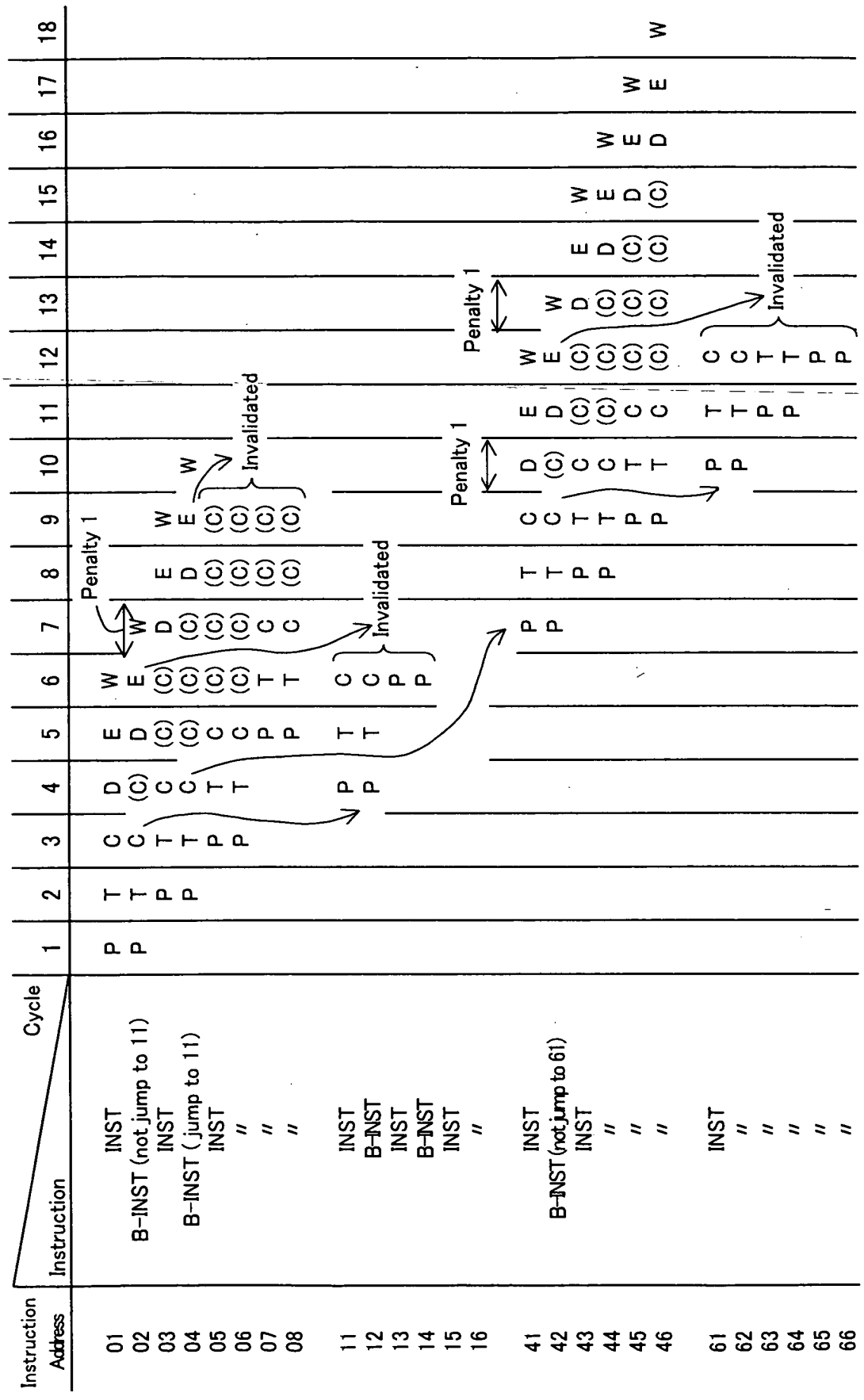

FIG. 11

At Cycle 6 of Route (3)

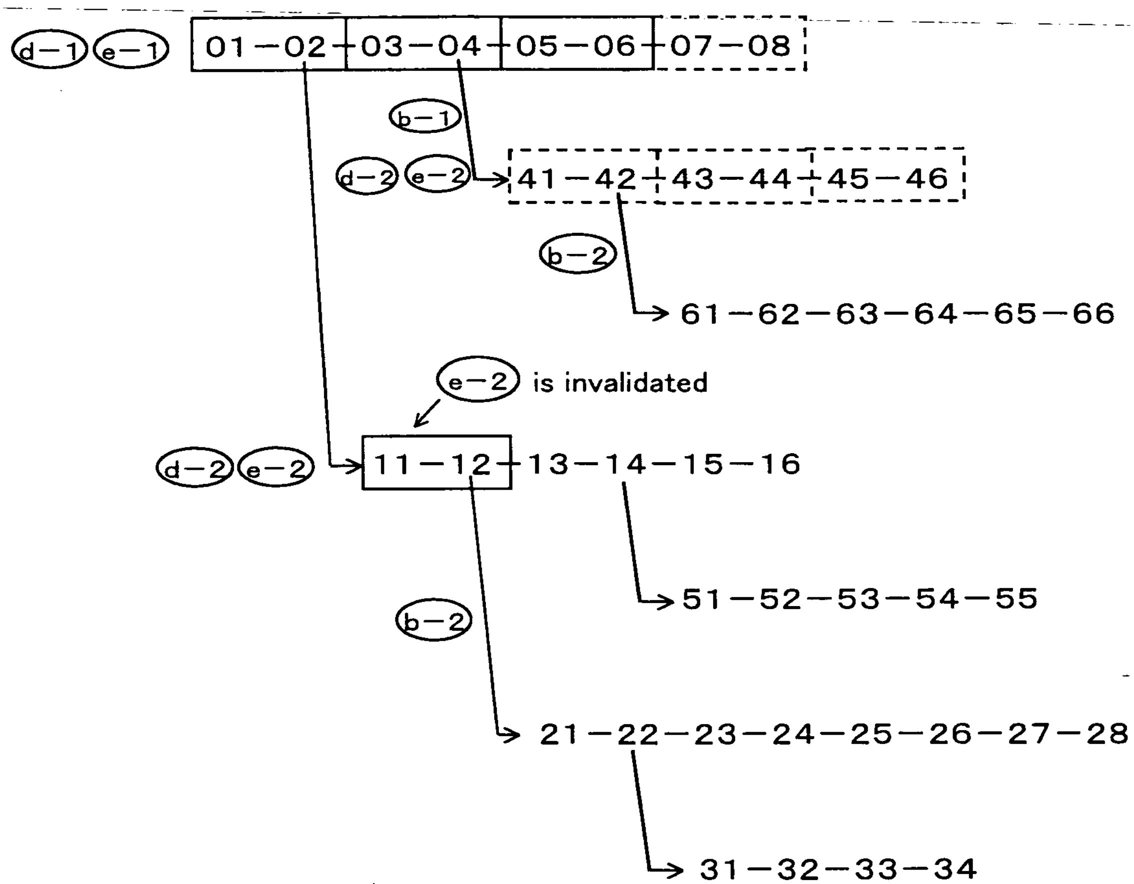

FIG. 12

Branching Route (4)

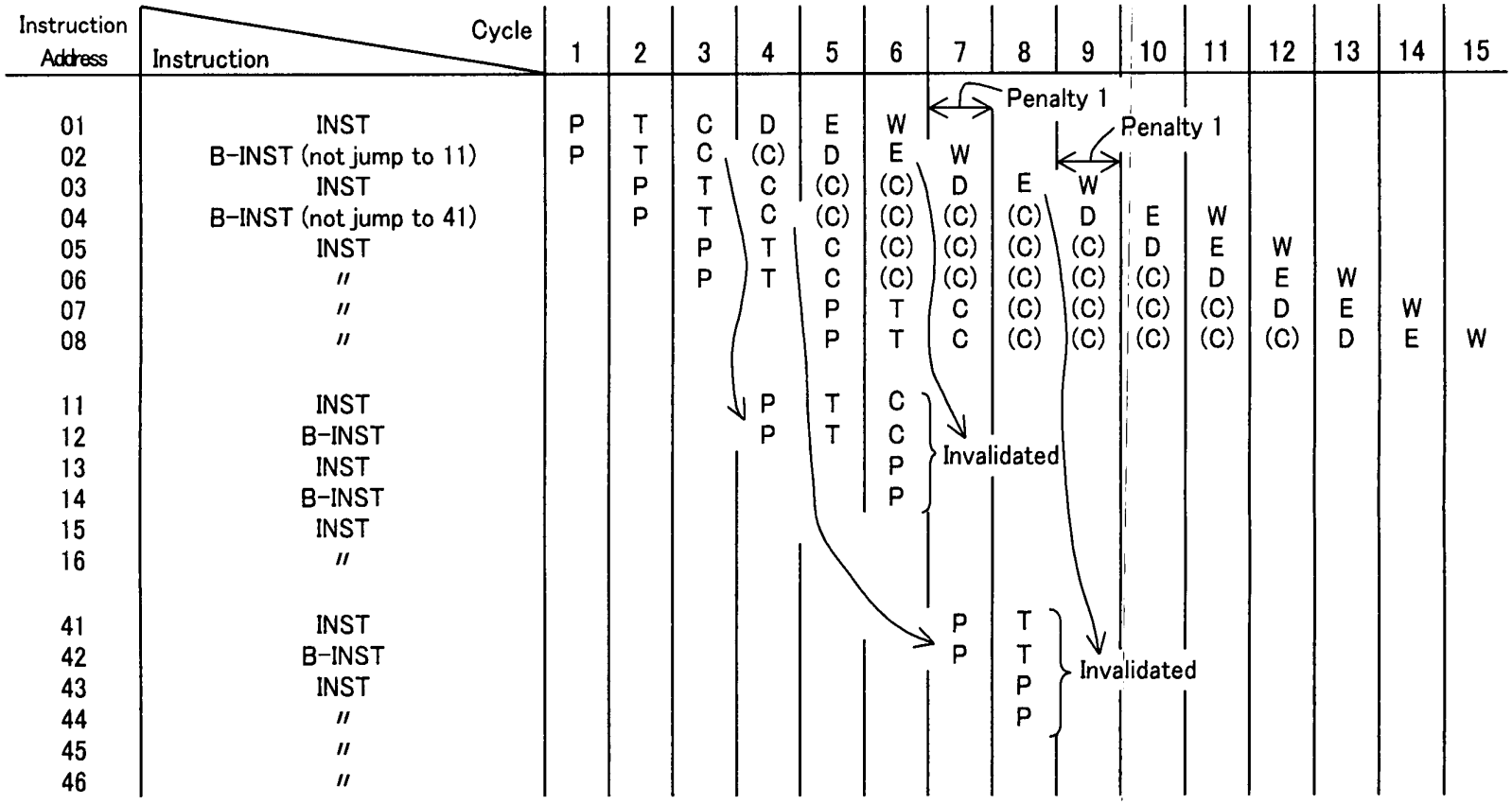

FIG. 13

Prior Art

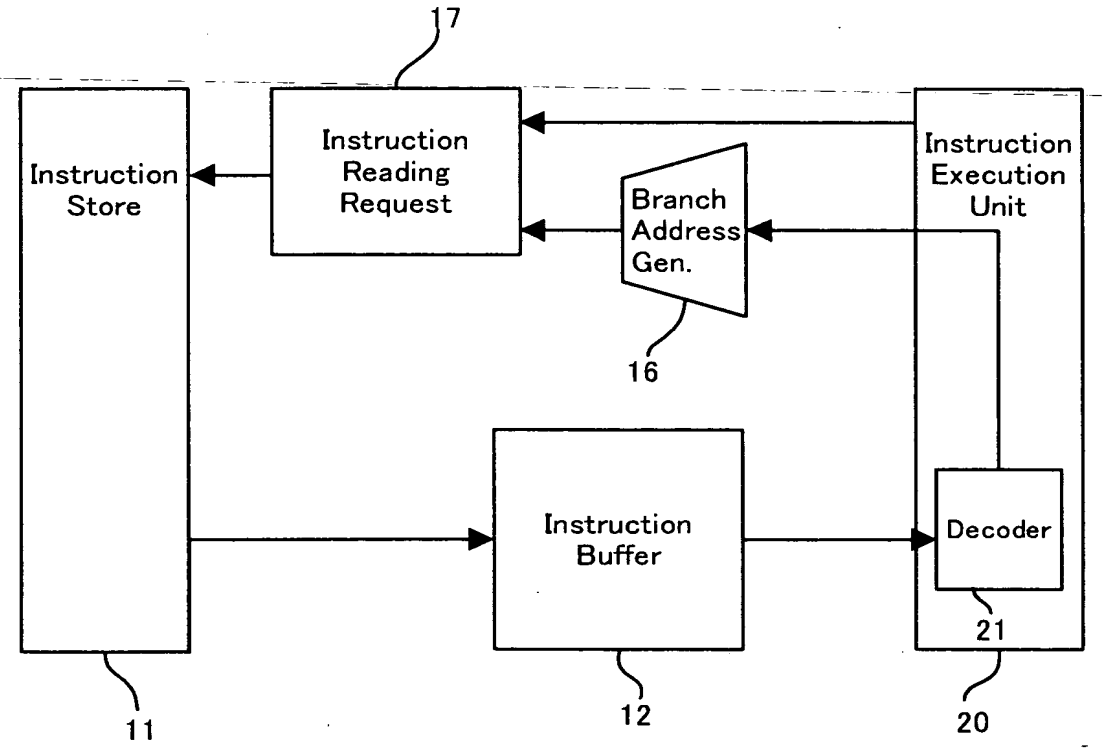

FIG. 14

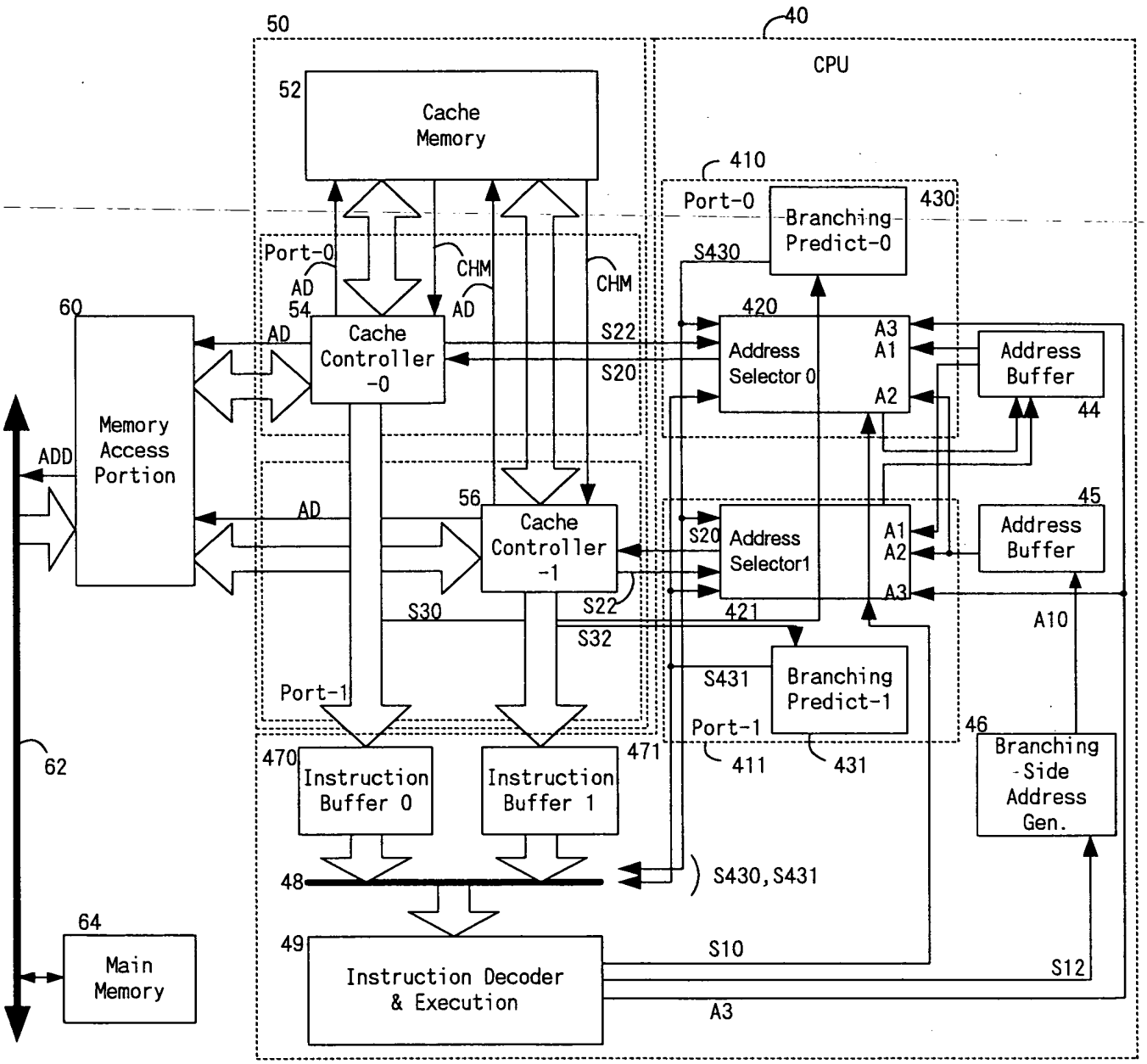
50
40
CPU
52
Cache Memory
410
Port-0
430
Branching-Predict-0
S430
Port-0
AD
54
CHM
AD
CHM
60
AD
Cache Controller -0
S22
S20
420
Address Selector 0
A3
A1
A2
Address Buffer
44
Memory Access Portion
ADD
AD
56
Cache Controller -1
S20
Address Selector1
A1
A2
A3
Address Buffer
45
S30
S22
S32
421
A10
S431
Branching Predict-1
Port-1
46
Port-1
411
431
Branching -Side Address Gen.
62
470
Instruction Buffer 0
Instruction Buffer 1
471
48
S430,S431
64
Main Memory
49
Instruction Decoder & Execution
S10
S12
A3

FIG. 15

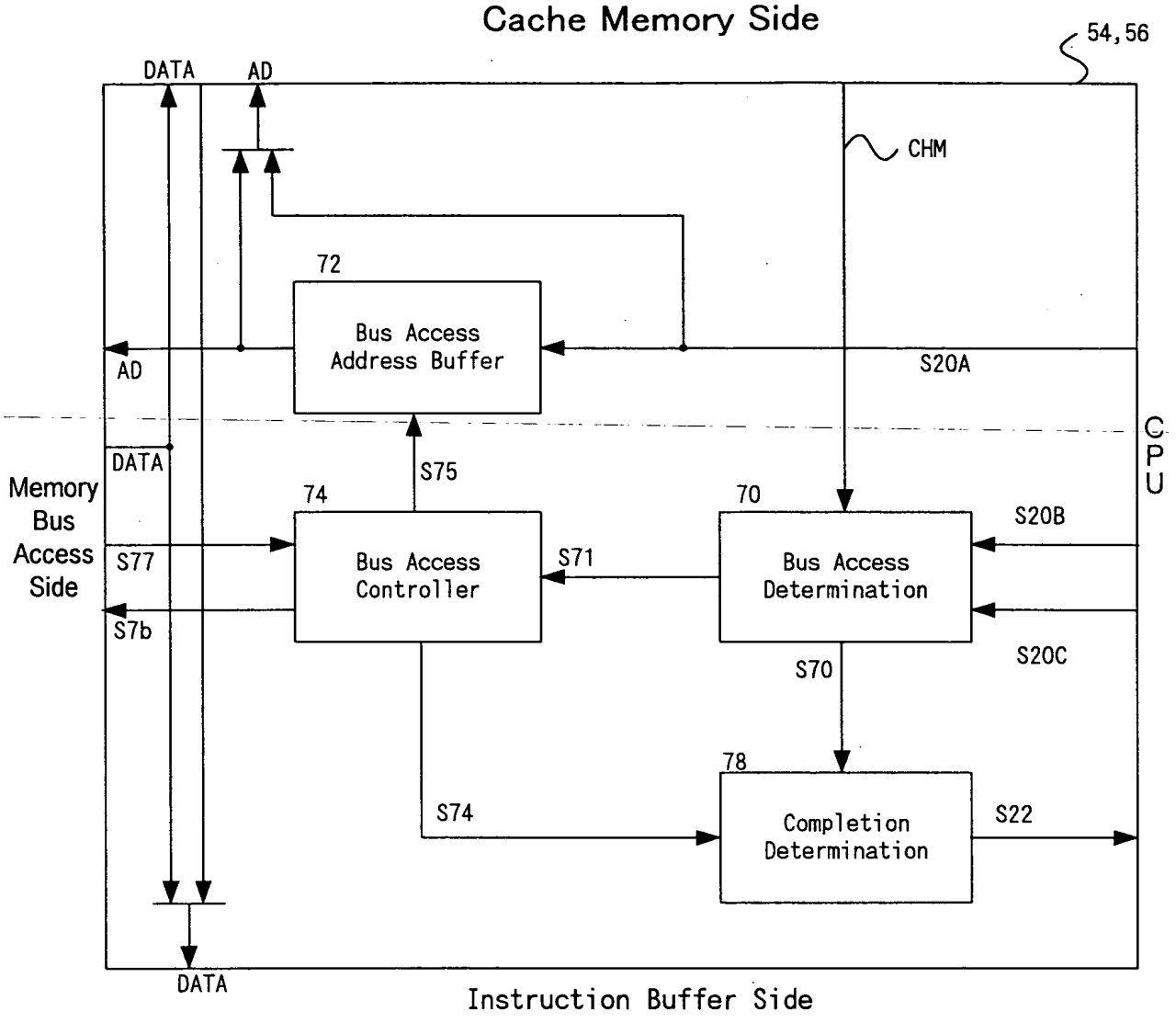

FIG. 16

First Control Example

	Branching direction not determined							
	Cache Hit		Memory Bus Access					
Predicted Branching Direction	Sequential Side	Target Side	Sequential Side		Target Side		Memory Bus Access after determined	
			Bus Access	Fetch	Bus Access	Fetch	S Sequential	T Target
Sequential Side	Miss	Miss	Yes	Yes	No	T	No	Yes
	Miss	Hit	Yes	Yes	No	Yes	No	No
	Hit	Miss	No	Yes	No	T	No	Yes
	Hit	Hit	No	Yes	No	Yes	No	No
Target Side	Miss	Miss	No	T	Yes	Yes	Yes	No
	Miss	Hit	No	T	No	Yes	Yes	No
	Hit	Miss	No	Yes	Yes	Yes	No	No
	Hit	Hit	No	Yes	No	Yes	No	No

FIG. 17

Second Control Example

	Branching direction not determined							
	Cache Hit		Memory Bus Access					
Predicted Branching Direction	Sequential Side	Target Side	Sequential Side		Target Side		Memory Bus Access after determined	
			Bus Access	Fetch	Bus Access	Fetch	S Sequential	T Target
Sequential Side	Miss	Miss	Yes	Yes	No	T	No	Yes
	Miss	Hit	Yes	Yes	No	Yes	No	No
	Hit	Miss	No	Yes	No	T	No	Yes
	Hit	Hit	No	Yes	No	Yes	No	No
Target Side	Miss	Miss	Yes	Yes	Yes	Yes	No	No
	Miss	Hit	Yes	Yes	No	Yes	No	No
	Hit	Miss	No	Yes	Yes	Yes	No	No
	Hit	Hit	No	Yes	No	Yes	No	No

FIG. 18

Third Control Example

	Branching direction not determined							
	Cache Hit		Memory Bus Access					
Predicted Branching Direction	Sequential Side	Target Side	Sequential Side		Target Side		Memory Bus Access after determined	
			Bus Access	Fetch	Bus Access	Fetch	S Sequential	T Target
Sequential Side	Miss	Miss	No	T	No	T	Yes	Yes
	Miss	Hit	No	T	No	Yes	Yes	No
	Hit	Miss	No	Yes	No	T	No	Yes
	Hit	Hit	No	Yes	No	Yes	No	No
Target Side	Miss	Miss	No	T	No	T	Yes	Yes
	Miss	Hit	No	T	No	Yes	Yes	No
	Hit	Miss	No	Yes	No	T	No	Yes
	Hit	Hit	No	Yes	No	Yes	No	No

FIG. 19

Fourth Control Example

	Branching direction not determined							
	Cache Hit		Memory Bus Access					
Predicted Branching Direction	Sequential Side	Target Side	Sequential Side		Target Side		Memory Bus Access after determined	
			Bus Access	Fetch	Bus Access	Fetch	S Sequential	T Target
Sequential Side	Miss	Miss	Yes	Yes	Yes	Yes	No	No
	Miss	Hit	Yes	Yes	No	Yes	No	No
	Hit	Miss	No	Yes	Yes	Yes	No	No
	Hit	Hit	No	Yes	No	Yes	No	No
Target Side	Miss	Miss	No	T	Yes	Yes	Yes	No
	Miss	Hit	No	T	No	Yes	Yes	No
	Hit	Miss	No	Yes	Yes	Yes	No	No
	Hit	Hit	No	Yes	No	Yes	No	No

FIG. 20

Embodiment

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	·	30	31	32	33	34	35	36
INST 01	P	T	C	D	E	E	E	W														
02		P	T	C	D	D	D	E	W													
03			P	T	C	C	C	D	E	W												
04				P	T	C	C	C	D	E	W											
05					P	T	C	C	C	D	E	W										
06						P	T	C	C	C	D	E	W									
07							P	T	C	C	C	D	E	W								
08								P	T	M	B	R	·	·	·	C	D	E	W			
09									P	T	M	B	B	B	·	·	C	D	E	W		
10										P	T	M	B	B	·	·	·	C	D	E	W	
11																	P	T	C	D	E	W
12																		P	T	C	D	E
51						P	T	M														
52							P	T	M													
53								P	T	M												

INST 01→INST 02→INST 03→INST 04→INST 05→INST 06→INST 07→INST 08→INST 09→
└→INST 51→INST 52→INST 53→INST 54→

(INST 03 is branching instruction, is predected not to branch, and does not branch is fact)

FIG. 21

Prior Art

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	·	28	29	30	·	46	47	48
INST 01	P	T	C	D	E	E	E	W														
02		P	T	C	D	D	D	E	W													
03			P	T	C	C	C	D	E	W										-		
04				P	T	C	C	C	D	E	W											
05					P	T	C	C	C	D	E	W										
06						P	T	C	C	C	D	E	W									
07							P	T	C	C	C	D	E	W								
08								P	T	M	B	B	B	B	·	R	·	·	·	C	D	E
09									P	T	M	B	B	B	·						C	D
10										P	T	M	B	B	·							C
11																					P	T
12																						P
51						P	T	M	B	R	·	·	·	·	·	C						
52							P	T	M	B	B	B	B	B	·	·	C					
53								P	T	M	B	B	B	B	·	·	·	C				

INST 01→INST 02→INST 03→INST 04→INST 05→INST 06→INST 07→INST 08→INST 09→
└→INST 51→INST 52→INST 53→INST 54→

(INST 03 is branching instruction, is predected not to branch, and does not branch is fact)